THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 23

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

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Ex parte JAMES S. BLONGREN

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Appeal No. 97-0582
Application 08/179,926[1]

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ON BRIEF

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Before THOMAS, KRASS and FLEMING, ***Administrative Patent Judges***.

FLEMING, ***Administrative Patent Judge***.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 1 through 20, all of the claims present in the application.

[1]Application for patent filed January 11, 1994.

The invention relates to computer system architectures, and more particularly to microprocessors that can execute multiple instructions sets. Appellants disclose on pages 11 and 12 of the specification that Figure 2 shows a simplified block diagram of a CPU that can execute both reduced instruction set computer (RISC) and complex instruction set computer (CISC) instructions. In particular, Figure 2 shows that instructions are fetched and supplied to a RISC instruction decoder (RISC ID 36) and a CISC instruction decoder (CISC ID 36). Either the decoded RISC instruction or the decoded CISC instruction is selected by MUX 46 and outputted to execute unit 48 for execution of the decoded instruction.

The independent claim 1 is reproduced as follows:

> 1. A central processing unit (CPU)for processing instructions from two separate instruction sets, said CPU comprising:
>
> > first instruction decode means for decoding instructions from a first instruction set, said first instruction set having a first encoding of instructions;
> >
> > second instruction decode means for decoding only a subset of instructions from a second instruction set, said second instruction set having a second encoding of instructions, said first encoding of instructions independent from said second encoding of instructions;
> >
> > select means, coupled to said first instruction decode means and said second instruction decode means, for selecting said decoded instruction from either said

first instruction decode means or from said second instruction decode means; and

execute means for executing decoded instructions selected by said select means, whereby instructions from both said first instruction set and said second instruction set are executed by said CPU.

The Examiner relies on the following references:

Onishi		3,764,988	Oct. 09, 1973
Bullions, III et al.	(Bullions)[2]	4,456,954	Jun. 26, 1984
Portanova et al.	(Portanova)	4,992,934	Feb. 12, 1991

Claims 1 through 5, 14 through 16 and 18 through 20 stand rejected under 35 U.S.C. § 103 as being unpatentable over Portanova and Onishi. Claims 6 through 13 and 17 stand rejected under 35 U.S.C. § 103 as being unpatentable over Portanova, Onishi and Bullions.

Rather than reiterate the arguments of Appellants and the Examiner, reference is made to the briefs[3] and answers[4] for the

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[2]In the answer as well as the supplemental answer, the Examiner invites us to consider an IBM technical disclosure as well as Iwata, U.S. Pat. No. 4,691,278. However, the Examiner has not rejected the claims based upon these references. Therefore, we find that these references are not properly before us for our consideration.

[3]Appellants filed an appeal brief on August 29, 1995. We will refer to this appeal brief as simply the brief. Appellants filed a reply appeal brief on November 29, 1995. We will refer to this reply appeal brief as the reply brief. The Examiner responded to the reply brief with a supplemental answer stating that the reply brief has been entered. Appellants filed a supplement to the brief on June 25, 1997. The Examiner responded

respective details thereof.

OPINION

We will not sustain the rejection of claims 1 through 20 under 35 U.S.C. § 103.

The Examiner has failed to set forth a ***prima facie*** case. It is the burden of the Examiner to establish why one having ordinary skill in the art would have been led to the claimed invention by the express teachings or suggestions found in the prior art, or by implications contained in such teachings or suggestions. ***In re Sernaker***, 702 F.2d 989, 995, 217 USPQ 1, 6 (Fed. Cir. 1983). "Additionally, when determining obviousness, the claimed invention should be considered as a whole; there is no legally recognizable 'heart' of the invention." ***Para-Ordnance Mfg. v. SGS Importers Int'l, Inc.***, 73 F.3d 1085, 1087, 37 USPQ2d 1237, 1239 (Fed. Cir. 1995), ***cert. denied,*** 117 S.Ct. 80 (1996)

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to the supplement to the brief with a second supplemental answer thereby entering the supplement to the brief into the record.

[4]The Examiner responded to the brief with an Examiner's answer, mailed November 9, 1995. We will refer to the Examiner's answer as simply the answer. The Examiner responded to the reply brief with a supplemental Examiner's answer, mailed August 16, 1996. We will refer to the Supplemental Examiner's answer as simply the supplemental answer. The Examiner responded to the supplement to the brief with a second supplemental Examiner's answer, mailed June 25 1997, by stating that no further arguments are necessary. The Examiner offered no other response.

citing W. L. Gore & Assocs., Inc. v. Garlock, Inc., 721 F.2d 1540, 1548, 220 USPQ 303, 309 (Fed. Cir. 1983), ***cert. denied***, 469 U.S. 851 (1984).

Appellants argue on pages 8 through 15 of the brief that Portanova and Onishi fail to suggest modifying Portanova to provide a CISC decoder in addition to Portanova's RISC decoder as recited in Appellants' claims. On page 4 of the answer, the Examiner argues that it would have been obvious to provide two instruction decoders because the use of two separate instruction decoders allows for simpler and more efficient design of the decoders.

The Federal Circuit states that "[t]he mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." ***In re Fritch***, 972 F.2d 1260, 1266 n.14, 23 USPQ2d 1780, 1783-84 n.14 (Fed. Cir. 1992), ***citing In re Gordon***, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984). "Obviousness may not be established using hindsight or in view of the teachings or suggestions of the inventor." ***Para-Ordnance Mfg.***, 73 F.3d at 1087, 37 USPQ2d at 1239, ***citing W. L. Gore***, 721 F.2d at 1551, 1553, 220 USPQ at 311, 312-13.

Upon a closer review of Portanova, we fail to find that Portanova suggests to those skilled in the art to provide an additional CISC decoder. Portanova teaches in column 1, lines 15-23, that although the development of CISC software is simpler and easier to use, the CISC hardware requires the use of very large scale integration resulting in a highly complex microprocessor hardware design. Portanova further teaches in column 1, lines 24-42, that RISC systems require simpler microprocessors, but require more functions to be done in software. In column 3, lines 44-56, Portanova teaches that the object of their invention is to provide a simple RISC architecture which eases the hardwired decoding of instructions which in turn speeds control paths but also can emulate CISC instruction sets. Portanova teaches in column 4, lines 18-34, that the Portanova RISC architecture responds to CISC instructions by addressing a corresponding one of a plurality of groups of RISC instructions, each corresponding to one of the complex instructions. Thus, Portanova teaches that the same RISC architecture may be use to process a CISC instruction so that the simpler and faster RISC hardware may be used for both instructions sets. From this teaching, Portanova leads those

skilled in the art away from using the more complex CISC instruction decoders which require the more complex hardware.

Turning to Onishi, we fail to find that Onishi suggests modifying Portanova with an additional CISC decoder. Onishi is not concerned with processing different instruction sets, but instead is concerned with improving the speed for processing branch instructions. Therefore, we find that neither Portanova nor Onishi provides any reason or suggestion to modify the Portanova RISC architecture to provide an additional CISC decoder to obtain the method or apparatus as claimed by Appellants.

We have not sustained the rejection of claims 1 through 20 under 35 U.S.C. § 103. Accordingly, the Examiner's decision is reversed.

REVERSED

JAMES D. THOMAS Administrative Patent Judge	)	
ERROL A. KRASS Administrative Patent Judge	)	BOARD OF PATENT APPEALS AND INTERFERENCES
MICHAEL R. FLEMING	)	

Administrative Patent Judge)

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